REMARKS

Claims 28-29, 31-38 and 40-52 remain in the present application. Claim 52 is added herein. Applicants respectfully submit that no new matter has been added as a result of the claim amendments. Applicants respectfully request further examination and reconsideration of the rejections.

Claim Rejections – 35 U.S.C. §103

Claims 28-29, 31-38 and 40-51

Claims 28-29, 31-38 and 40-51 are rejected in the present Office Action under 35 U.S.C. §103(a) as being unpatentable over United States Patent Number 3,805,247 to Zucker et al. (referred to herein as "Zucker") in view of United States Patent Number 5,949,982 to Frankeny et al. (referred to herein as "Frankeny"). Applicants respectfully submit that the embodiments of the present invention as recited in Claims 28-29, 31-38 and 40-51 are not rendered obvious by Zucker in view of Frankeny for the following reasons.

Applicants respectfully direct the Examiner to independent Claim 28, which recites a system comprising (emphasis added):

> a plurality of memory resources;
> a plurality of peripheral resources;
> a plurality of processors;
> a memory controller coupled to said plurality of processors and said plurality of memory resources, wherein said memory controller comprises a first resource controller for controlling access of said plurality of processors to said plurality of memory resources, wherein said first resource controller is further operable to implement a first bus for enabling first communication between a first processor of said plurality of processors and a first memory resource of said plurality of memory resources, wherein said first resource controller is further operable to implement a second bus for enabling second communication between a

second processor of said plurality of processors and a second memory resource of said plurality of memory resources, wherein said first resource controller is further operable to implement said first and second buses for enabling said first communication to occur independently of said second communication, and wherein said first communication occurs simultaneously with said second communication; and

a peripheral controller coupled to said plurality of processors and said plurality of peripheral resources, wherein said peripheral controller comprises a second resource controller for controlling access of said plurality of processors to said plurality of peripheral resources, and wherein said first resource controller is further operable to implement respective buses for coupling said plurality of processors to said plurality of peripheral resources.

Independent Claims 37 and 46 recite elements similar to independent Claim 28. Claims 29, 31-36, 38, 40-45 and 47-51 depend from their respective independent Claims and recite further elements of the claimed invention.

Page 4 of the rejection states that "Zucker however does not expressly state that simultaneous access to different memories is performed." Accordingly, Applicants respectfully submit that Zucker fails to teach or suggest the elements of "wherein said first resource controller is further operable to implement a first bus for enabling first communication between a first processor of said plurality of processors and a first memory resource of said plurality of memory resources," "wherein said first resource controller is further operable to implement a second bus for enabling second communication between a second processor of said plurality of processors and a second memory resource of said plurality of memory resources" and "wherein said first communication occurs simultaneously with said second communication" as recited in independent Claim 28.

Applicants respectfully submit that Frankeny, either alone or in combination with Zucker, also fails to teach or suggest the elements of "wherein said first resource controller is further operable to implement a first bus for enabling first communication between a first processor of said plurality of processors and a first memory resource of said plurality of memory resources," "wherein said first resource controller is further operable to implement a second bus for enabling second communication between a second processor of said plurality of processors and a second memory resource of said plurality of memory resources" and "wherein said first communication occurs simultaneously with said second communication" as recited in independent Claim 28. As described in the present application, a first resource controller is operable to implement a first bus for enabling first communication between a first processor of the plurality of processors and a first memory resource of the plurality of memory resources. The first resource controller is further operable to implement a second bus for enabling second communication between a second processor of the plurality of processors and a second memory resource of the plurality of memory resources. The first communication occurs simultaneously with the second communication.

In contrast to the claimed embodiments, Applicants understand Frankeny to teach simultaneous communication in both directions over a bi-directional interface between a device and a cross-bar switch (Abstract; col. 3, lines 56-59). In this manner, Frankeny teaches simultaneous communication between *two* components, e.g., a device and cross-bar switch, using a *single* interface (e.g.,

the bi-directional interface coupling the device and the cross-bar switch). Applicants respectfully submit that simultaneous communication between two components as taught by Frankeny is very different from simultaneous communication between *four* components (e.g., a first processor and a first memory resource, and a second processor and a second memory resource) using *two* buses as claimed. Accordingly, Applicants reiterate that Frankeny, either alone or in combination with Zucker, also fails to teach or suggest the elements of "wherein said first resource controller is further operable to implement a first bus for enabling first communication between a first processor of said plurality of processors and a first memory resource of said plurality of memory resources," "wherein said first resource controller is further operable to implement a second bus for enabling second communication between a second processor of said plurality of processors and a second memory resource of said plurality of memory resources" and "wherein said first communication occurs simultaneously with said second communication" as recited in independent Claim 28.

For these reasons, Applicants respectfully submit that independent Claim 28 is not rendered obvious by Zucker in view of Frankeny, thereby overcoming the 35 U.S.C. §103(a) rejection of record. Since independent Claims 37 and 46 recite elements similar to those discussed above with respect to independent Claim 28, Applicants respectfully submit that independent Claims 37 and 46 also overcome the 35 U.S.C. §103(a) rejection of record. Since dependent Claims 29, 31-36, 38, 40-45 and 47-51 recite further elements of the invention claimed in

their respective independent Claims, Applicants respectfully submit that Claims 29, 31-36, 38, 40-45 and 47-51 are also not rendered obvious by Zucker in view of Frankeny. Therefore, Applicants respectfully submit that Claims 28-29, 31-38 and 40-51 are allowable.

Claim 52

Applicants respectfully submit that Zucker fails to teach or suggest the elements of "wherein said memory controller is further operable to enable each processor of said plurality of processors to perform, in parallel, respective portions of a plurality of tasks" as recited in independent Claim 52. As described in the present application, a memory controller is operable to enable each processor of a plurality of processors to perform, in parallel, respective portions of a plurality of tasks. For example, as shown in Figures 5A through 5E of the instant application, first processor "P_1" performs a first portion of task "B" (e.g., portion "B_1") in parallel with the performance of a second portion of task "A" (e.g., portion "A_2") by second processor "P_2" (see, for example, lines 18-25 of page 7 of the instant application).

In contrast to the claimed embodiments, Applicants fail to find any teaching or suggestion in Zucker of a processor performing a portion of a task as claimed. Additionally, Applicants fail to find any teaching or suggestion in Zucker of a plurality of processors each performing a respective portion of a plurality of tasks as claimed. Further, Applicants fail to find any teaching or suggestion in Zucker of a plurality of processors each performing a respective portion of a

plurality of tasks *in parallel* as claimed. Accordingly, Applicants reiterate that Zucker fails to teach or suggest the elements of "wherein said memory controller is further operable to enable each processor of said plurality of processors to perform, in parallel, respective portions of a plurality of tasks" as recited in independent Claim 52.

Applicants respectfully submit that Frankeny, either alone or in combination with Zucker, fails to cure the deficiencies of Zucker discussed herein. More specifically, Applicants respectfully submit that Frankeny, either alone or in combination with Zucker, also fails to teach or suggest the elements of "wherein said memory controller is further operable to enable each processor of said plurality of processors to perform, in parallel, respective portions of a plurality of tasks" as recited in independent Claim 52.

For these reasons, Applicants respectfully submit that Claim 52 is not rendered obvious by Zucker in view of Frankeny.

CONCLUSION

Applicants respectfully submit that Claims 28-29, 31-38 and 40-52 are in condition for allowance and Applicants earnestly solicit such action from the Examiner.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

MURABITO, HAO & BARNES LLP

Dated: 11 / 25 / 2009 /BMF/

Bryan M. Failing
Registration No. 57,974

Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060